DTCO Flow for Air Spacer Generation and its Impact on Power and Performance at N7

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I. Introduction

The integration of process simulations with device and circuit simulations through design-technology co-optimization (DTCO) is essential for the successful design of future semiconductor devices and technologies [1]. In this manuscript, we describe a novel DTCO flow and apply it to study the impact of spacers with an air gap (AG), known as air spacers (ASs) on the circuit-level power and performance at the 7 nm node, using a 5-stage ring oscillator (RO) as an example circuit. The effective spacer capacitance, C_{eff}, is a limiting factor in the achievable frequency $f \propto 1/C_{\text{eff}}$ and power $P \propto C_{\text{eff}}$ of the oscillator [2].

It is essential to understand process variations and the limitations in reducing the capacitance imposed by the fabrication of the AS, when designing the RO circuit. The main fabrication parameters which impact the AG geometry are the sticking coefficient s and the thickness of the conformally-deposited SiN layer t_c which determines the width of the trench prior to non-conformal deposition. Since s is directly related to the fabrication condition in the chemical vapor deposition (CVD) chamber, such as pressure and temperature [3], this provides a direct link between circuit-level performance and the fabrication conditions.

II. Simulation Flow

The simulation of the fabrication-induced variation in the RO performance using physics-based models is not feasible, since physical process models require a time-intensive Monte Carlo (MC) ray tracing and level set (LS) approach. Therefore, we first perform a set of physical simulations in order to generate an analytical model for non-conformal CVD [4] which is based on these physics-based models, as implemented in ViennaPS [5]. This analytical model is subsequently applied in the full DTCO flow in order to study the impact of the fabrication parameters on the circuit performance. The critical steps in the workflow, as shown in Fig. 1, are described in this section.

A. Physical Topography Simulation

The physical simulation for the generation of the AG in the spacer is based on a LS powered topography simulator, together with top-down MC ray tracing for the simulation of non-conformal CVD [6]. Initially, a conformal layer of width t_c is deposited in the spacer trench, which can be modeled using physical or analytical approaches. After this, a non-conformal CVD is simulated using a single-particle approach, where the particle has a specific sticking coefficient s which describes its propensity to adsorb onto the surface [7]. Higher s values represent higher non-linearities which ensure that the gap is pinched off at the top. Several physical simulations are performed while varying t_c and s in order to subsequently devise a fast analytical model using the generated geometries.

B. Geometrical Description of the Air Gap

The principal aim of the analytical model is to reproduce the geometrical shape of the AG inside the spacer by reproducing the pinch-off height (POh), bottom height (Bh), and air gap width (AGw) from the physical CVD model (Fig. 2). This model also applies a linear interpolation for the air gap's geometrical parameters for s and t_c values which have not been simulated with the physical model. The air gap's shape is represented using a superellipse centered at $(0, 0)$ with radii r_x and r_y along the x and y axes, respectively, using the equation

$$y = \pm r_y \sqrt[4]{1 - |x/r_x|^4}. \quad (1)$$

C. Analytical Topography Simulation

In our DTCO flow, the complete AS is generated by first assuming a fully-filled SiN spacer and then performing a Boolean operation to remove the AG geometry from the spacer region. The AG geometry follows Eq. (1) while its vertical placement depends on the physically-modeled values of POh and Bh. This method allows to reproduce the physical AS model with high accuracy, as shown in Fig. 3, while requiring a fraction of the simulation time. The analytical model showed a speedup of about $100\times$, which is consistent with our previous studies [4].

D. Capacitance Extraction

The capacitance across the generated AS is calculated by solving the Poisson equation, which allows to extract a relationship between the capacitance and the chosen fabrication parameters. Ultimately, the calculated capacitance is used to extract an effective relative permittivity ε_{eff} of the AS, which contains an AG surrounded by SiN. The range of ε_{eff} we observe for the tested fabrication conditions is from about 4.2 to 5.7, as shown in Fig. 4, while a pure SiN spacer exhibits an ε_{eff} of 7.4.

E. Power-Performance Analysis

With the calculated ε_{eff} values, a power-performance analysis (PPA) of a 5-stage inverter RO logic cell is performed assuming varying fabrication conditions. The SPICE model cards are extracted automatically from the TCAD transistor characteristics and the parasitics network is calculated from the full three-dimensional (3D) RO cell using a field solver. Applying this method, any change in capacitance can be captured in a consistent manner [1], [8]. As expected, the results clearly show that the introduction of an air gap (AG) results in an improvement in the power and achievable frequency in all cases, as shown in Fig. 5.

III. Results and Discussion

We apply our developed DTCO framework on two fabrication flows, both of which are compatible with complementary semiconductor-metal-oxide (CMOS) technology. For one, the air spacer is formed prior to the deposition of middle of line (MOL) contacts (pre-MOL) [9] and for the second one the air spacer is formed after the deposition of MOL contacts (post-MOL) [2]. From Fig. 3 we note that both flows provide a similar air gap width, while the post-MOL-generated AG is shifted slightly up, due to the pinch-off location being slightly higher. A minimum conformal layer thickness of 2.5 nm was chosen because it was found that this allows for the pinch-off to stay within the spacer region. Otherwise, it may encroach into the inter-layer dielectric (ILD) layer between the MOL contacts.

The most significant impact on the spacer's effective relative permittivity is the AG width. This parameter is highly driven by the thickness of the conformally-deposited SiN. As can be observed from Fig. 4 the lowest permittivity is achieved when the sticking coefficient is high and the conformal layer thickness is low. These two factors essentially mean that the conformal deposition should set the width of the air gap, while the non-conformal deposition should only close the generated trench.

Finally, we observe the impact of the AS on a 5-stage inverter RO circuit using PPA, which is summarized in Fig. 5. We note that the inclusion of the air gap improves the performance by about 15 % in the worst case. With the presented framework, we are able to apply DTCO studies all the way from 3D physical process simulations through to geometric analysis of the spacer's topography and finally to thorough device and circuit analysis.

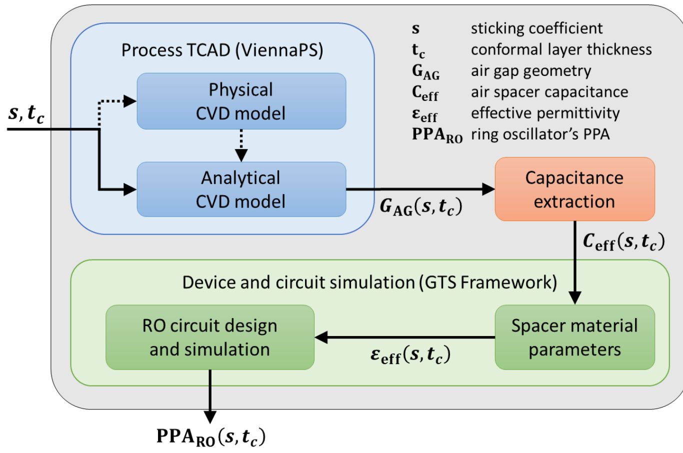

Fig. 1. Flowchart showing the presented DTCO workflow (solid arrow) for AS generation for a 5-stage inverter RO logic cell. The dotted arrow shows the development of the analytical model, which is based on a calibrated physical model. The main input parameters are the sticking coefficient s and conformal SiN layer thickness t_c, which are used to generate the air spacer geometry G_{AS}. The impact of the studied fabrication parameters (s, t_c) on the circuit power and performance are then provided using a PPA chart.

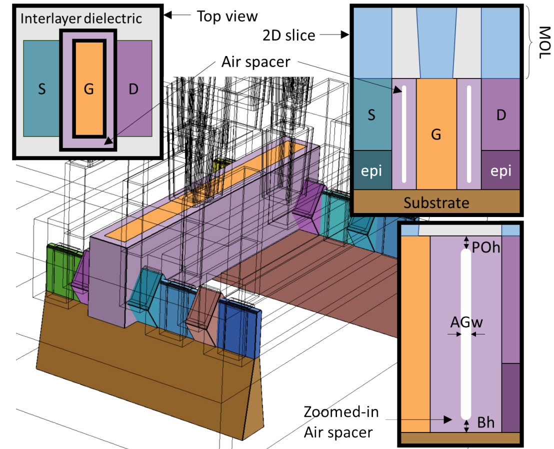

Fig. 2. Inverter cell with highlighted gate line and spacer regions. The insets show the spacer structure between source (S) and drain (D) regions, encircling the gate (G), below the MOL contacts. On the bottom right, the air spacer is shown with typical measurements for the pinch-off height (POh), bottom height (Bh) and the air gap width (AGw). These physical parameters are used to define the geometry of the air spacer G_{AS}.

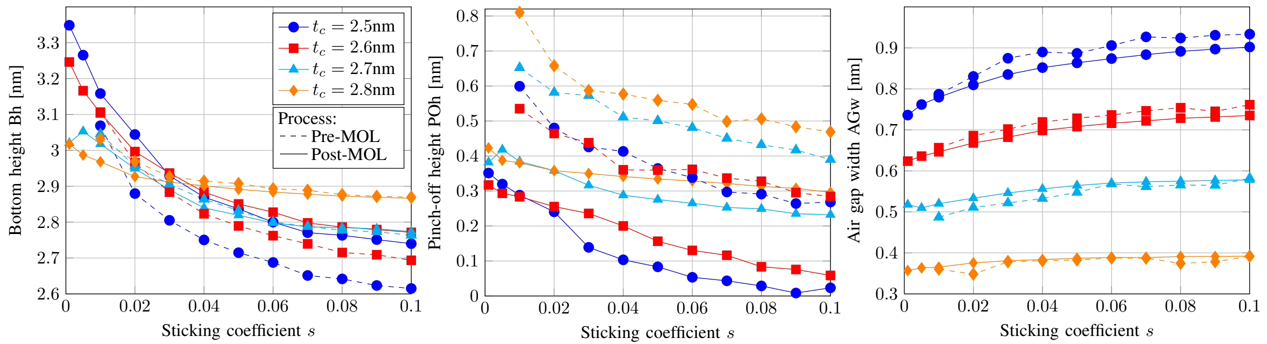

Fig. 3. Impact of s and t_c on the shape of the resulting air spacer geometry, including the bottom height (Bh), pinch-off height (POh), and the air gap width (AGw), as shown in Fig. 2. The symbols and lines show the results using the physical and analytical CVD models, respectively, while the dashed and solid lines show the results using the pre-MOL and post-MOL processes, respectively. We note that the analytical model is designed to replicate the physical model, while a linear interpolation is used to obtain the results between the physically-derived values. A clear impact of the two parameters is evident in all modeled scenarios.

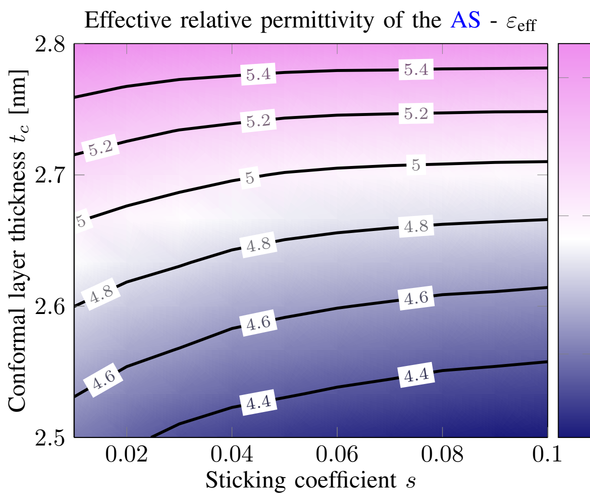

Fig. 4. The impact of the sticking coefficient s and conformal layer thickness t_c during air gap formation on the effective relative permittivity ε_{eff} of the air spacer using the post-MOL fabrication flow. We have also observed that the pre-MOL flow shows very similar results with ε_{eff} ranging from about 4.16 to 5.66 as s and t_c are varied. Therefore, increasing s and reducing t_c leads to lowest ε_{eff} values.

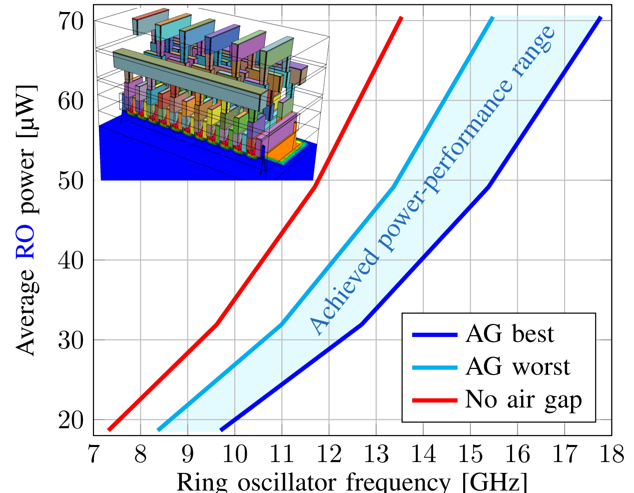

Fig. 5. Achieved power and performance for the RO with no air gap (AG) and with an AG under best and worst process conditions. The best condition corresponds to an ε_{eff} of 4.2 when $(s, t_c) = (0.1, 2.5\,\text{nm})$. The worst condition has $\varepsilon_{\text{eff}} = 5.7$ when $(s, t_c) = (0.02, 2.8\,\text{nm})$ in the pre-MOL process. The case with no air gap corresponds to a completely filled SiN spacer. The inset shows the full RO cell.

[1] G. Rzepa *et al.*, in IRPS 2021. DOI:10.1109/irps46558.2021.9405172
[2] K. Cheng *et al.*, *IEEE Transactions on Electron Devices*, vol. 67, no. 12, pp. 5355–5361, 2020. DOI:10.1109/ted.2020.3031878
[3] N. Cheimarios *et al.*, *Archives of Computational Methods in Engineering*, vol. 28, no. 2, pp. 637–672, 2020. DOI:10.1007/s11831-019-09398-w
[4] L. Filipovic and X. Klemenschits, in SISPAD 2021. DOI:10.1109/sispad54002.2021.9592595
[5] X. Klemenschits *et al.*, “ViennaPS - Vienna process simulation library,” [Online]. Available: https://github.com/ViennaTools
[6] X. Klemenschits, “Emulation and Simulation of Microelectronic Fabrication Processes,” Doctoral dissertation, TU Wien, Vienna, Austria, 2022.
[7] T. S. Cale and G. B. Raupp, *Journal of Vacuum Science & Technology B*, vol. 8, no. 6, p. 1242, 1990. DOI:10.1116/1.584901
[8] “GTS Cell Designer,” [Online]. Available: http://www.globaltcad.com/celldesigner
[9] K. Cheng *et al.*, in *IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 444–447. DOI:10.1109/iedm.2016.7838436